

Figure 1 (Prior Art)

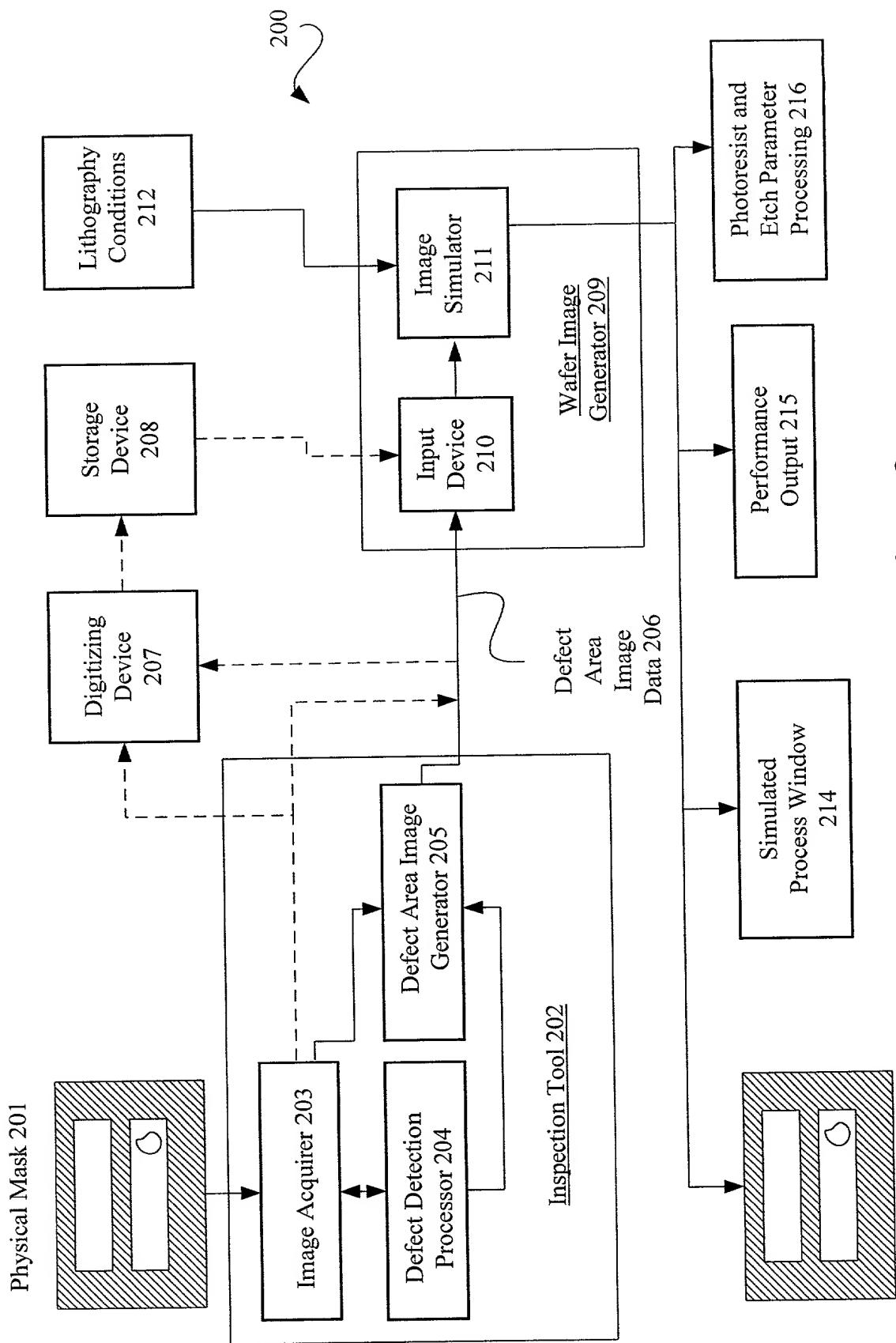


Figure 2

Simulated Wafer Image 213

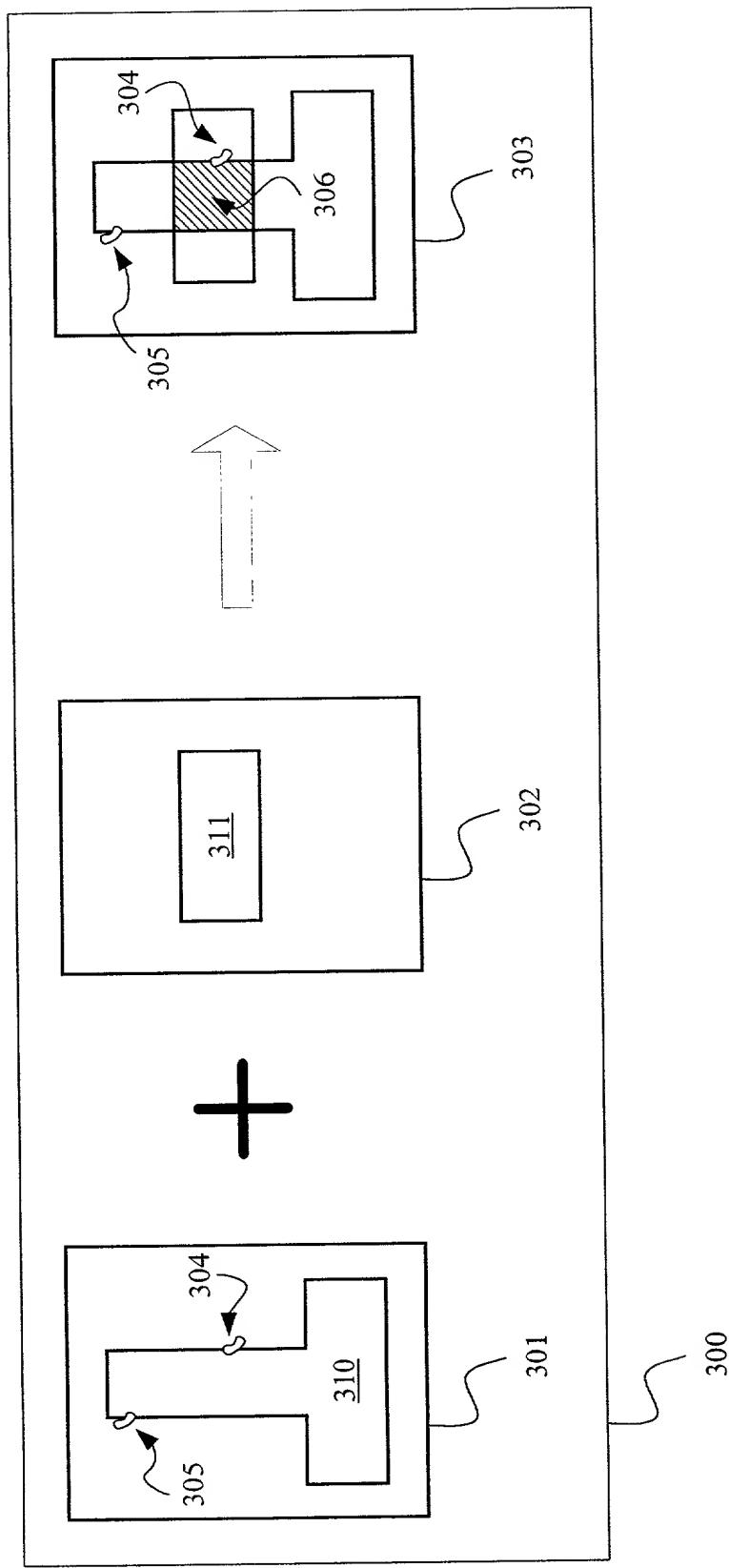
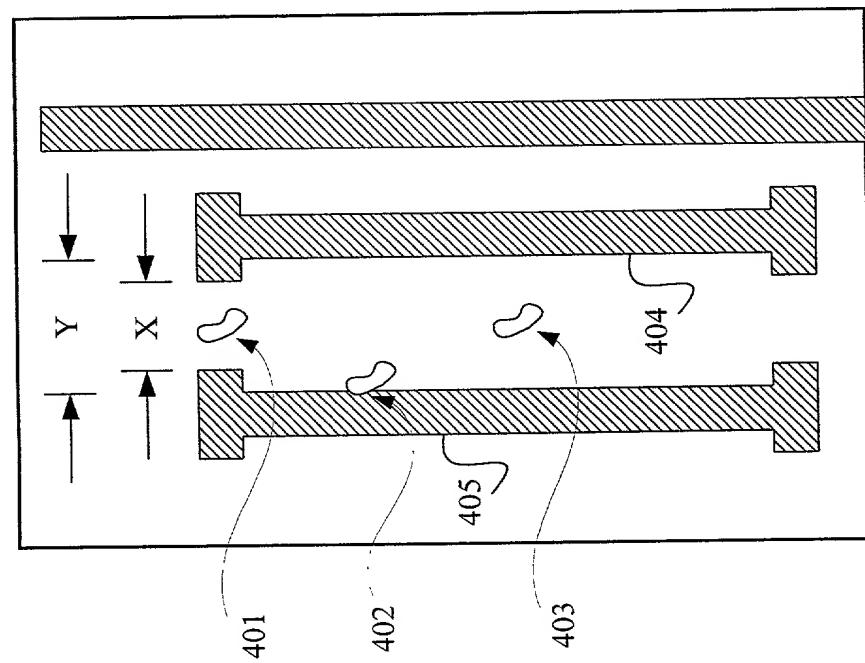
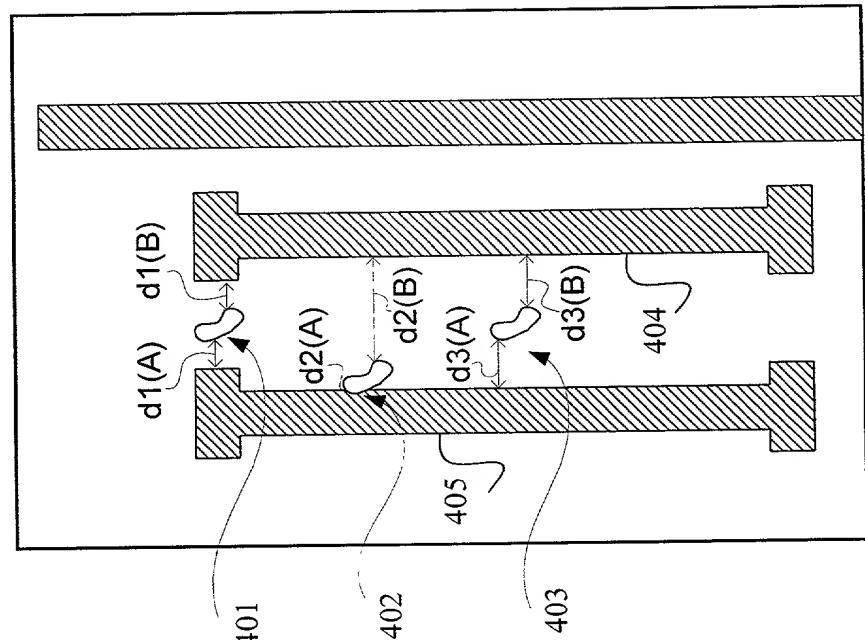


Figure 3



400
Figure 4A



400
Figure 4B

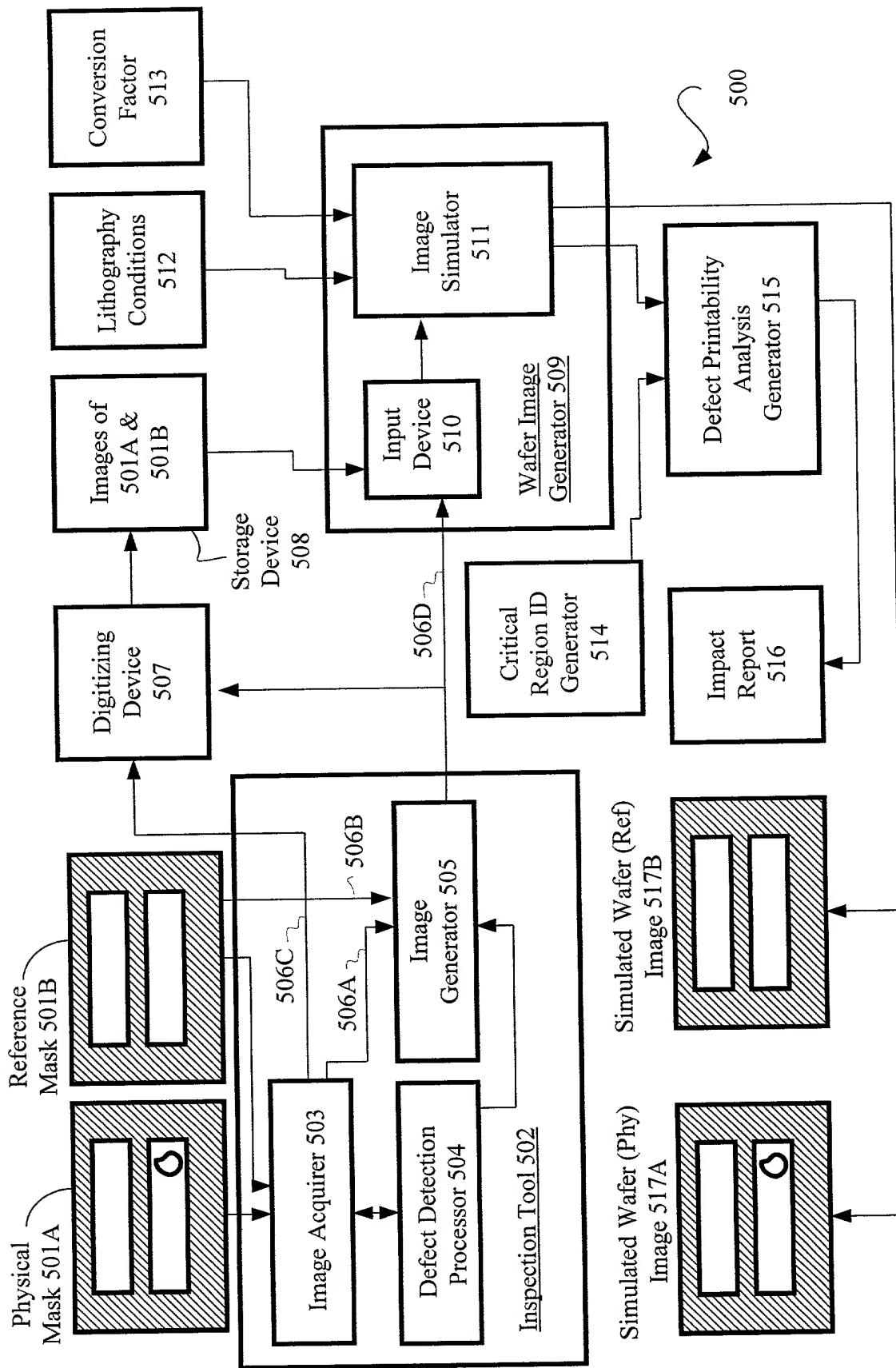


Figure 5

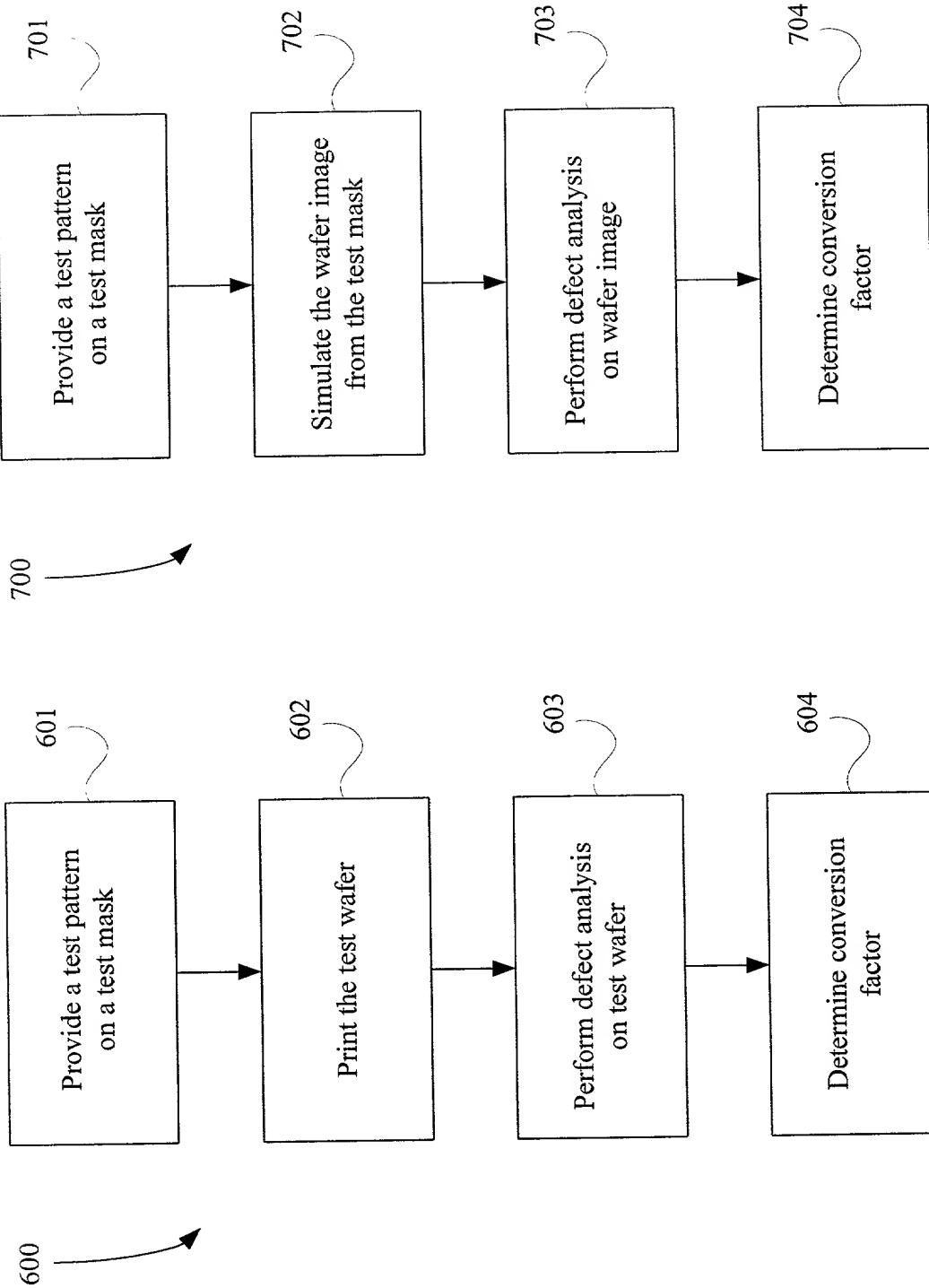


Figure 6

Figure 7

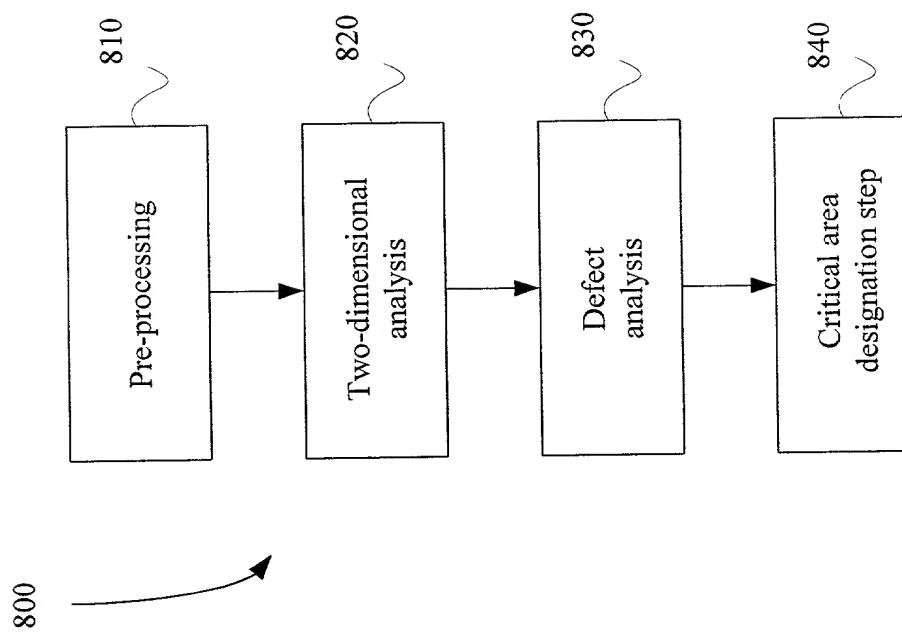


Figure 8A

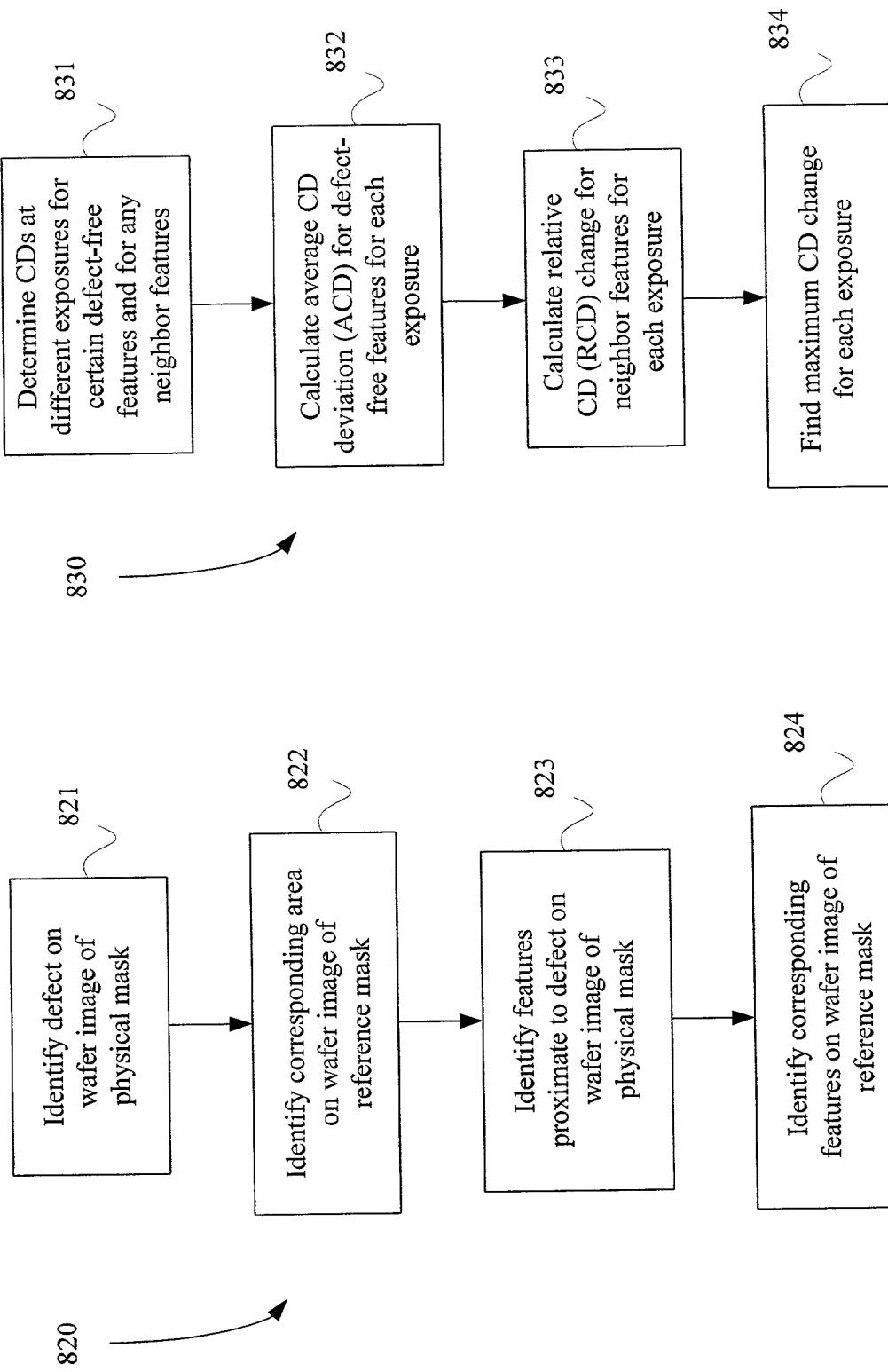
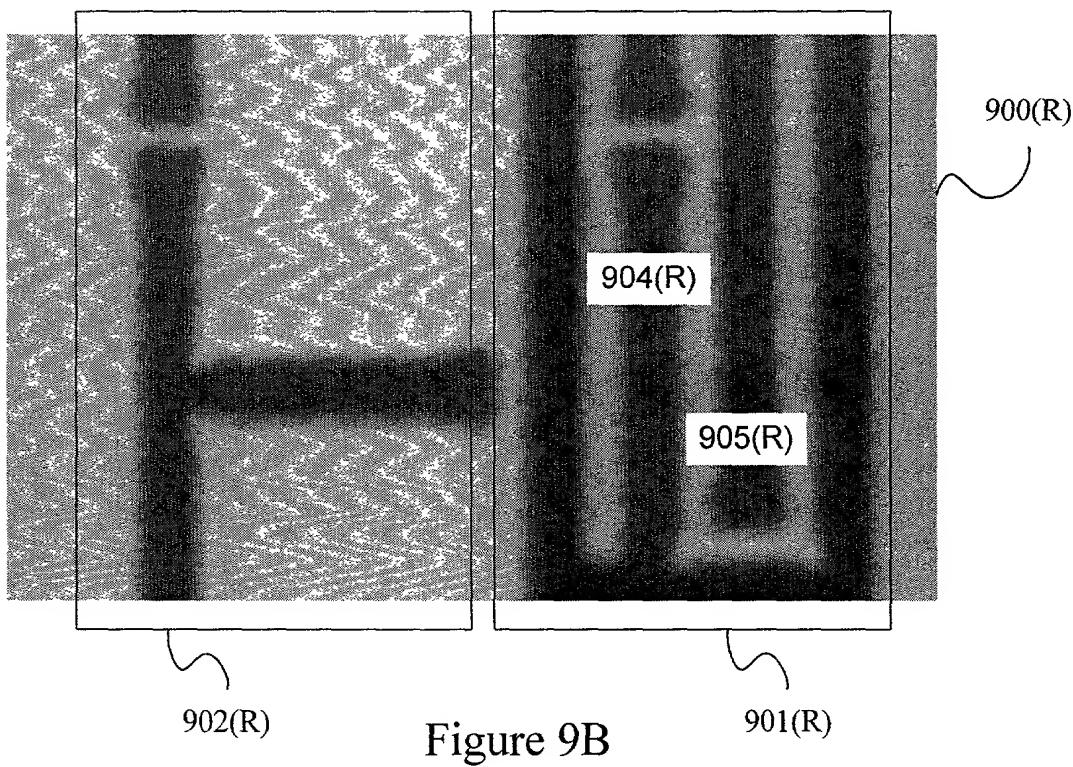
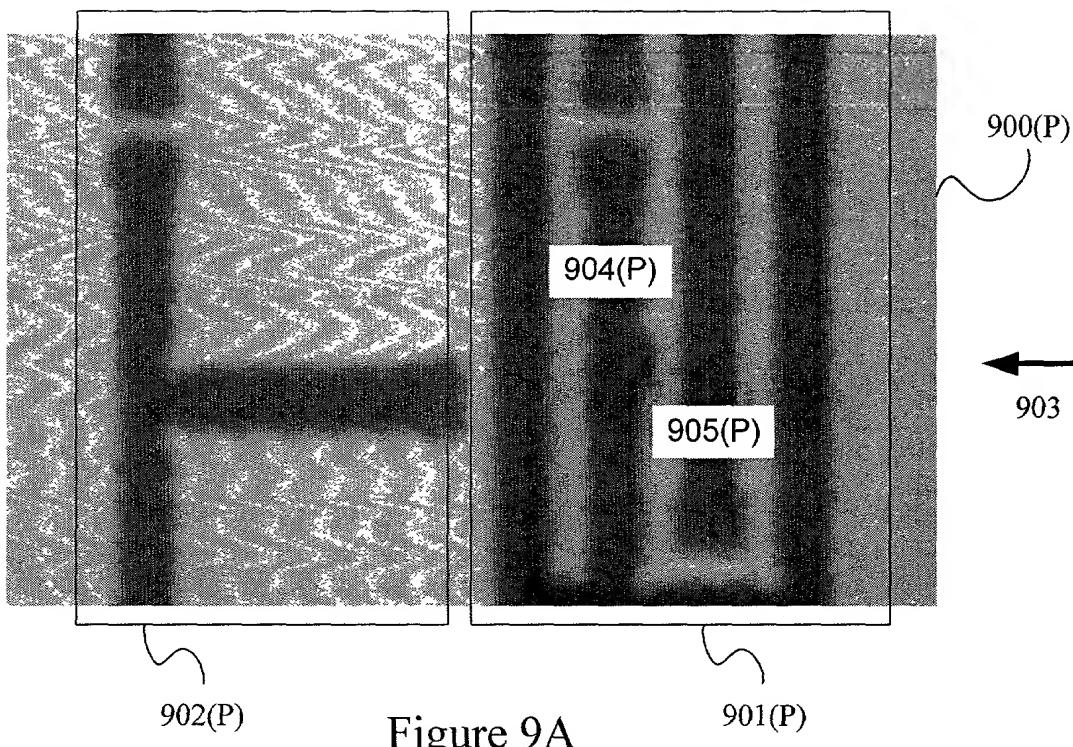


Figure 8B

Figure 8C



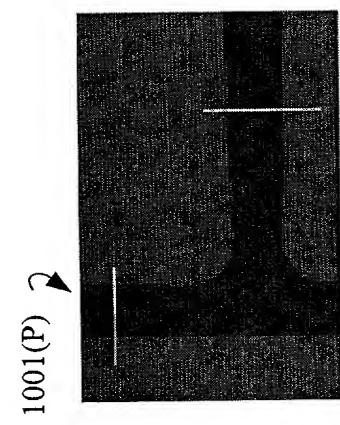


Figure 10A(1)

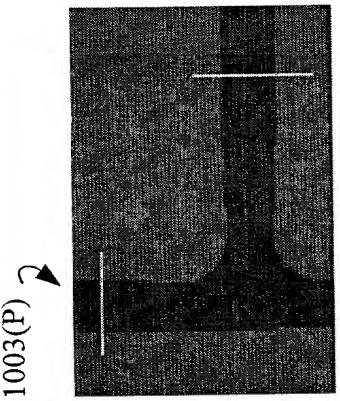


Figure 10A(2)

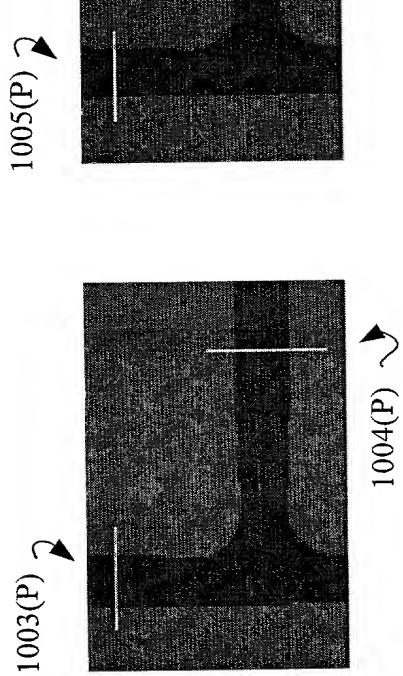


Figure 10A(3)

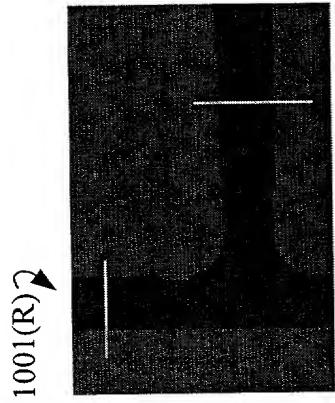


Figure 10B(1)

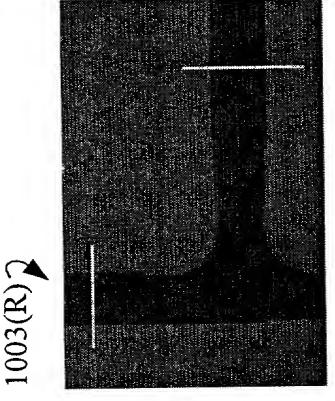


Figure 10B(2)

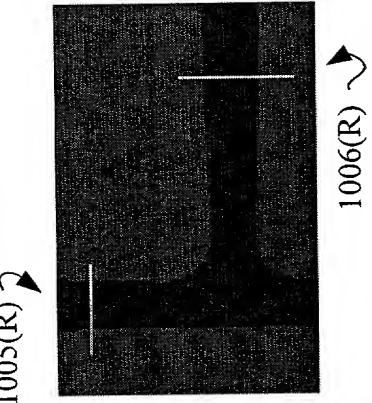


Figure 10B(3)

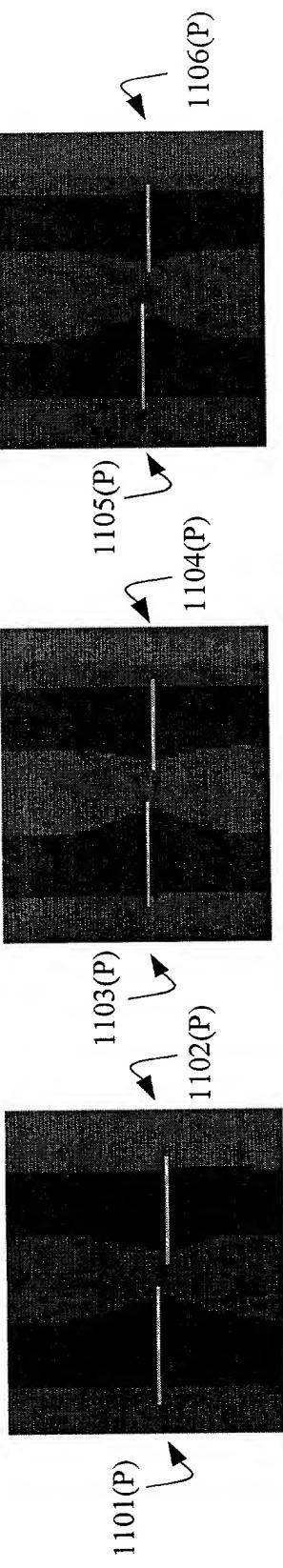


Figure 11A(1)

Figure 11A(2)

Figure 11A(3)

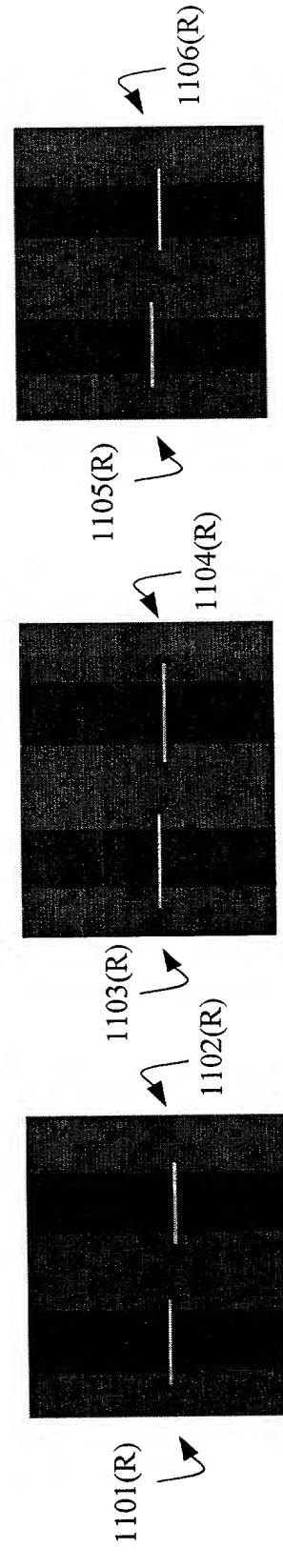


Figure 11B(1)

Figure 11B(2)

Figure 11(3)

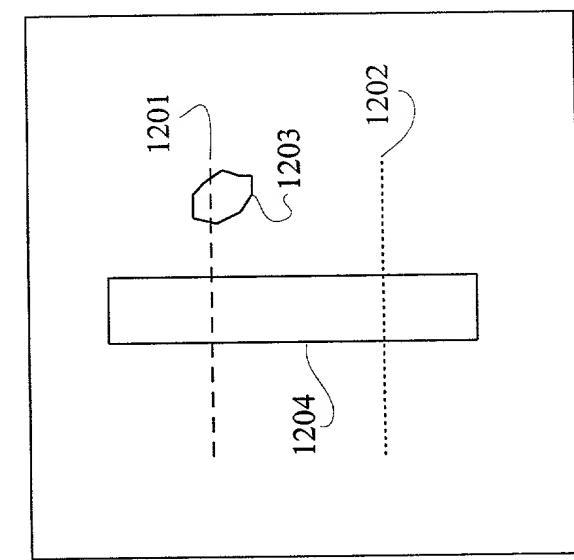


Figure 12A

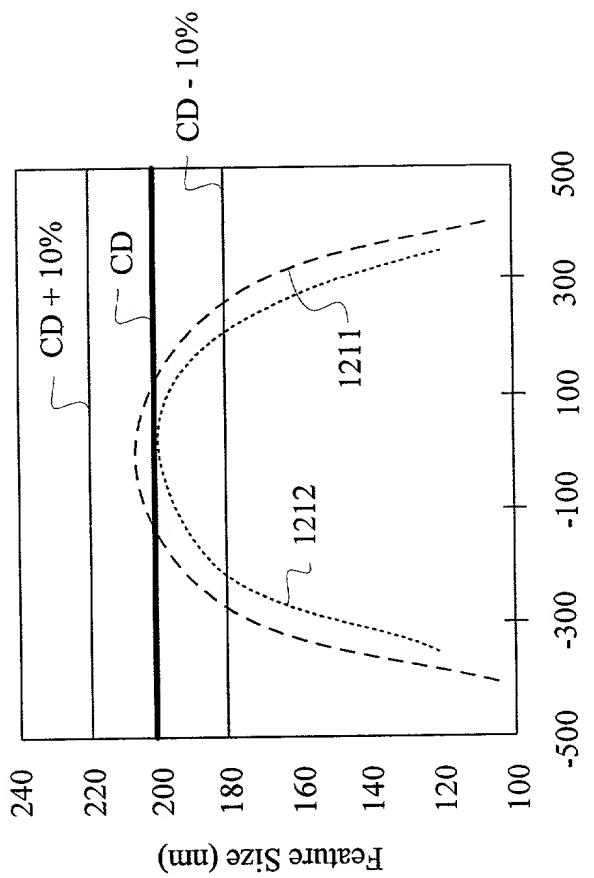


Figure 12B

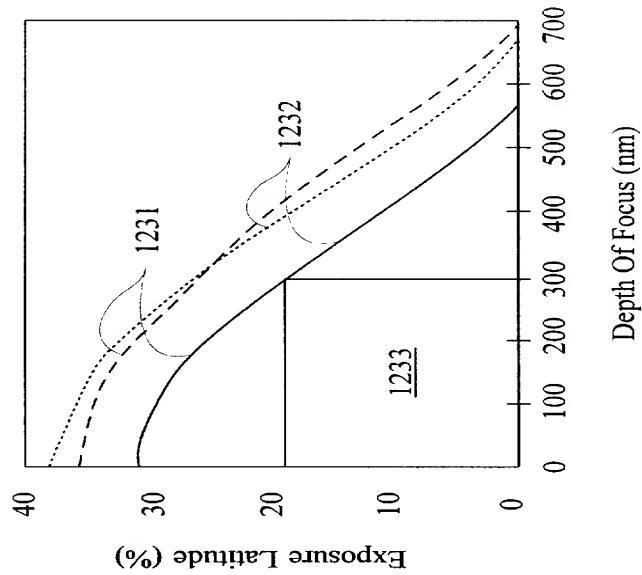


Figure 12D

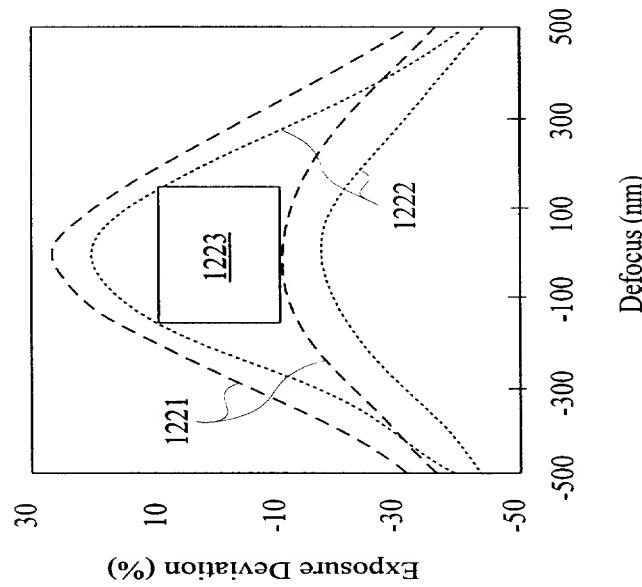


Figure 12C

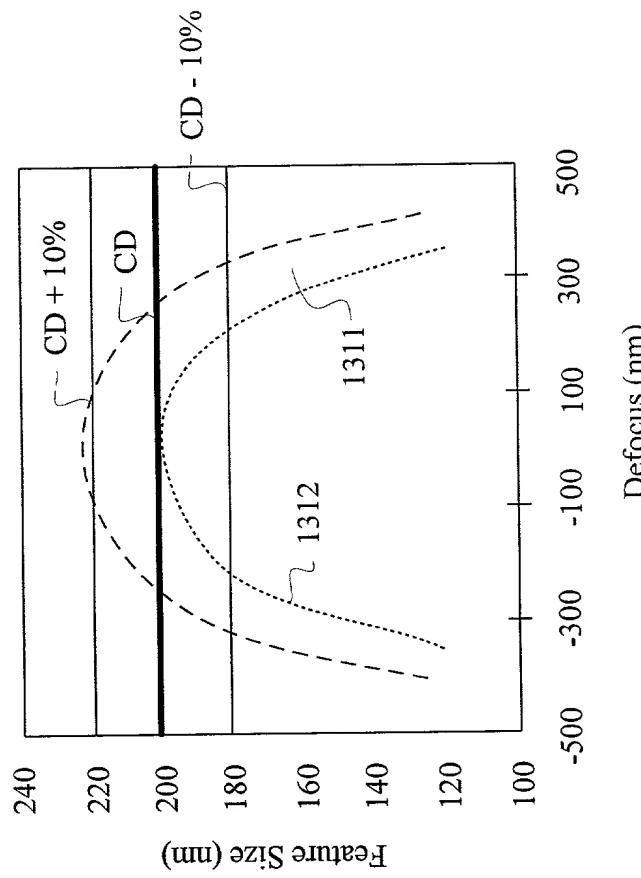


Figure 13B

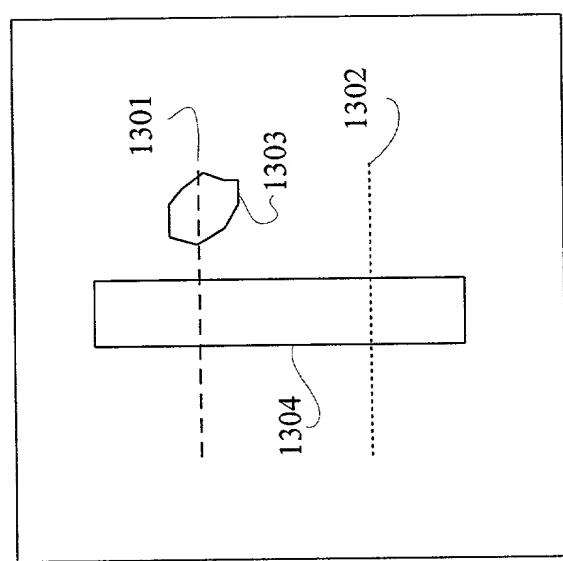


Figure 13A

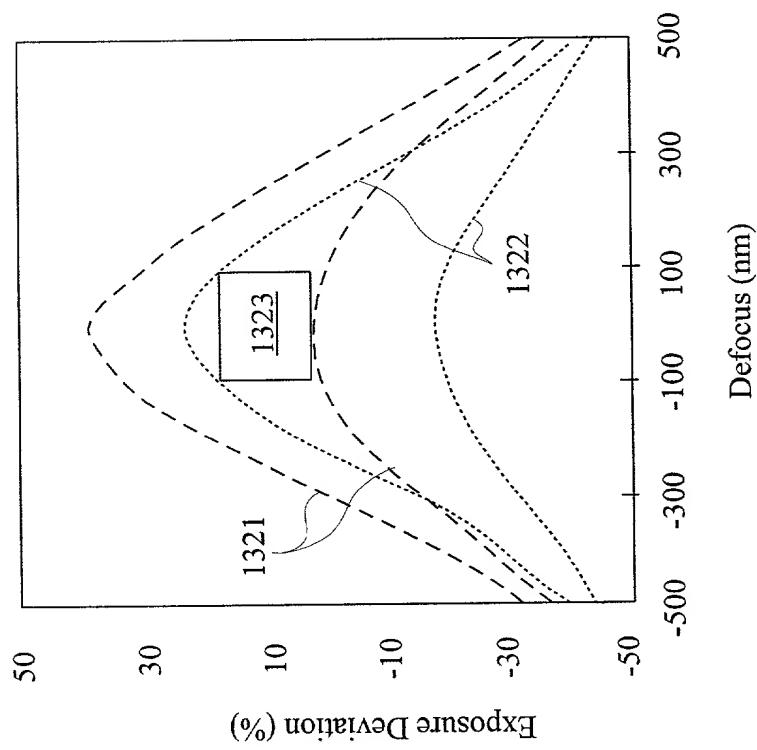


Figure 13C

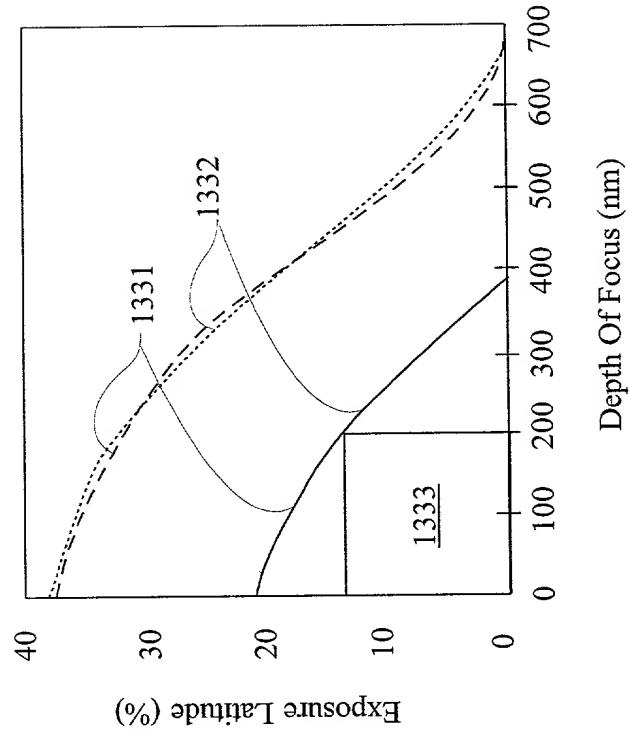


Figure 13D

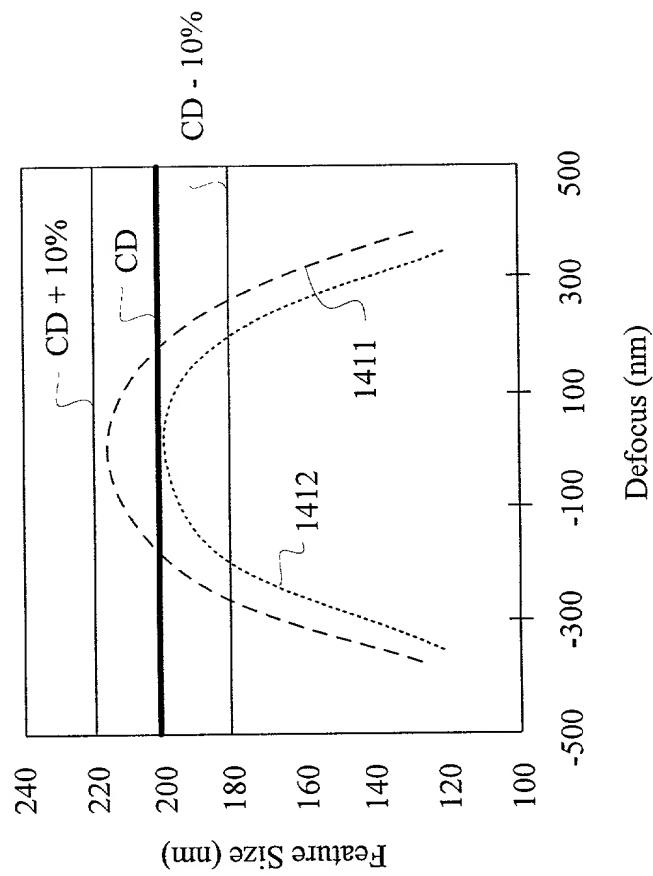


Figure 14B

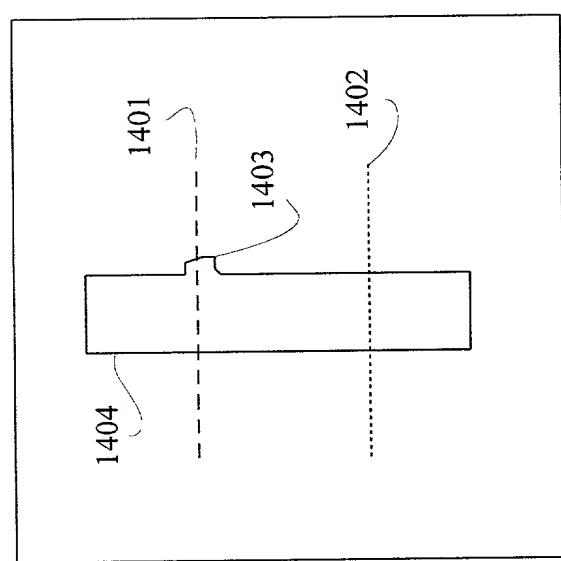


Figure 14A

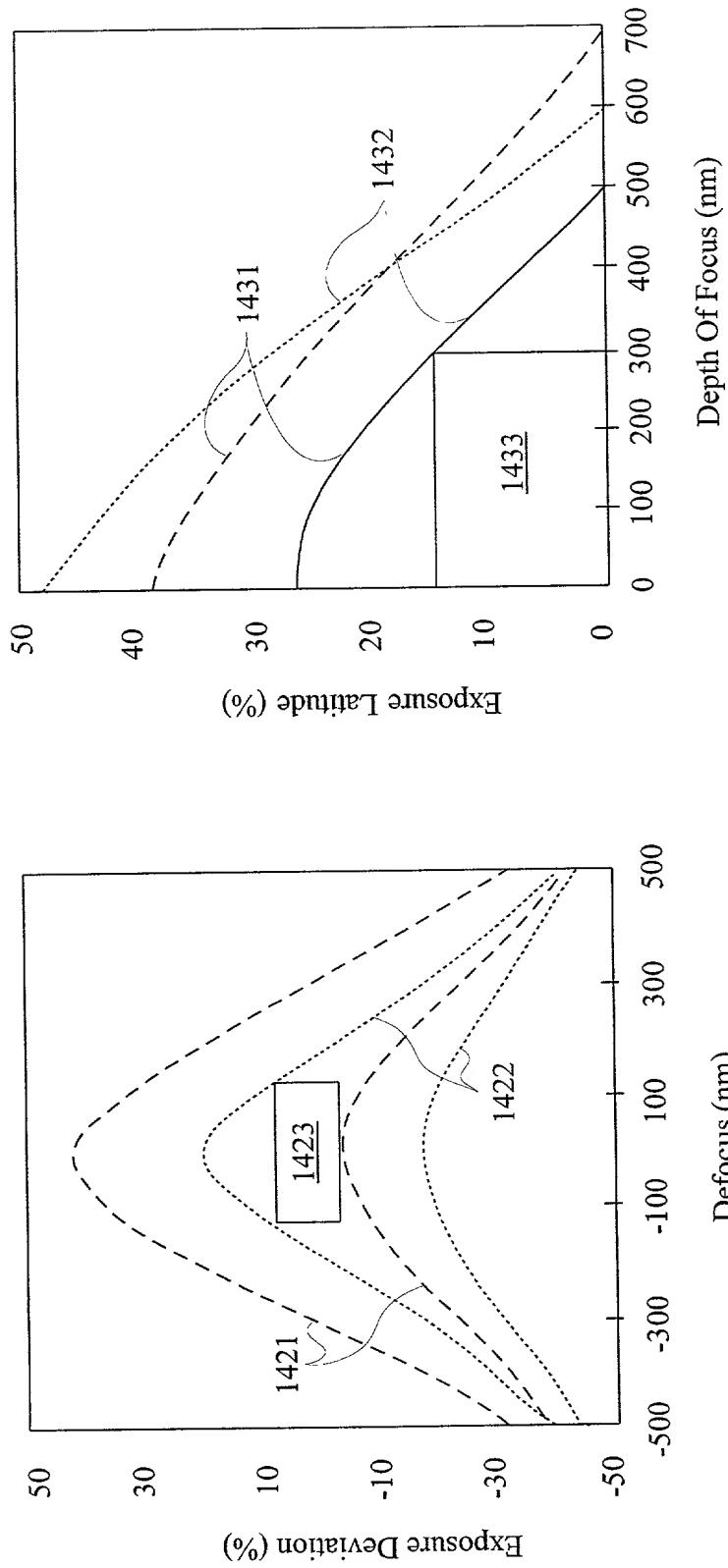


Figure 14D

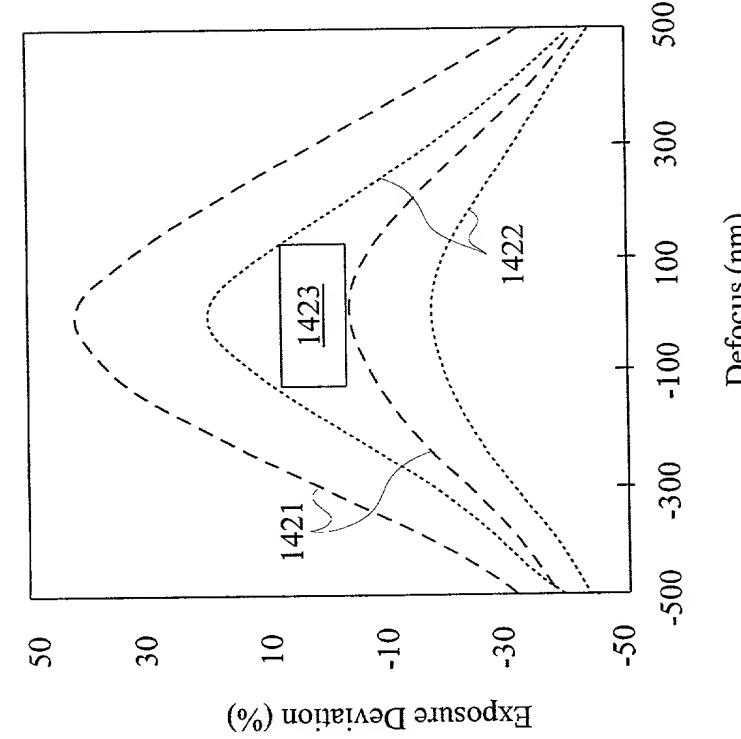


Figure 14C

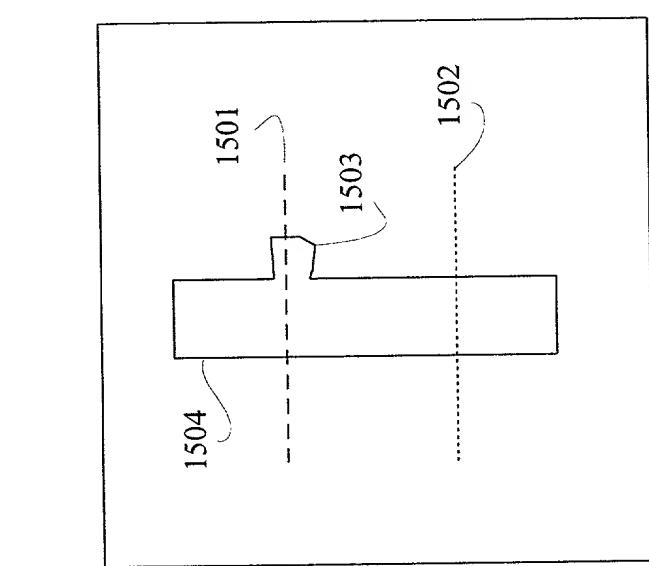


Figure 15A

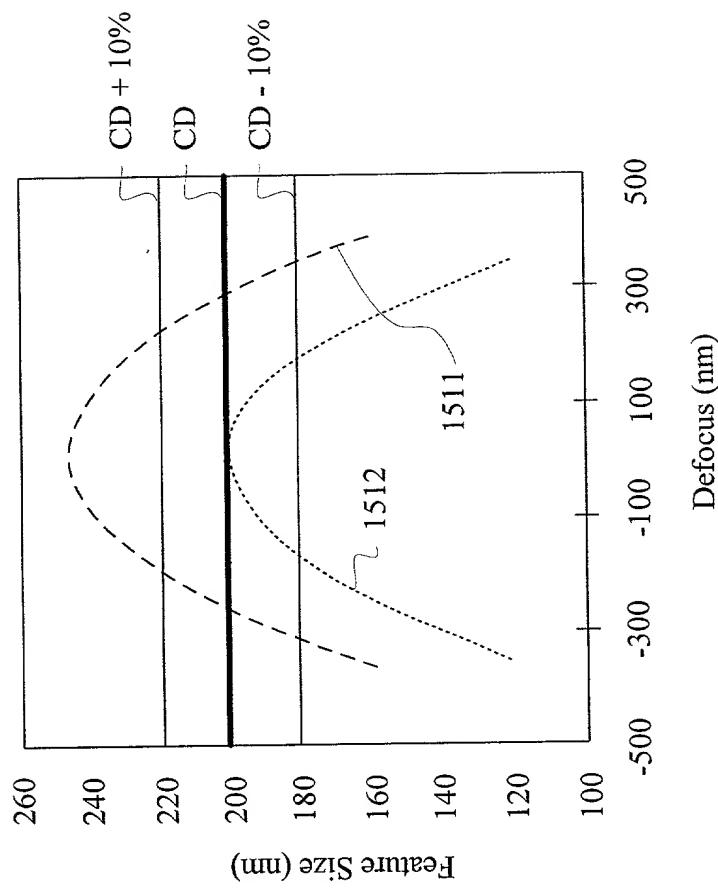


Figure 15B

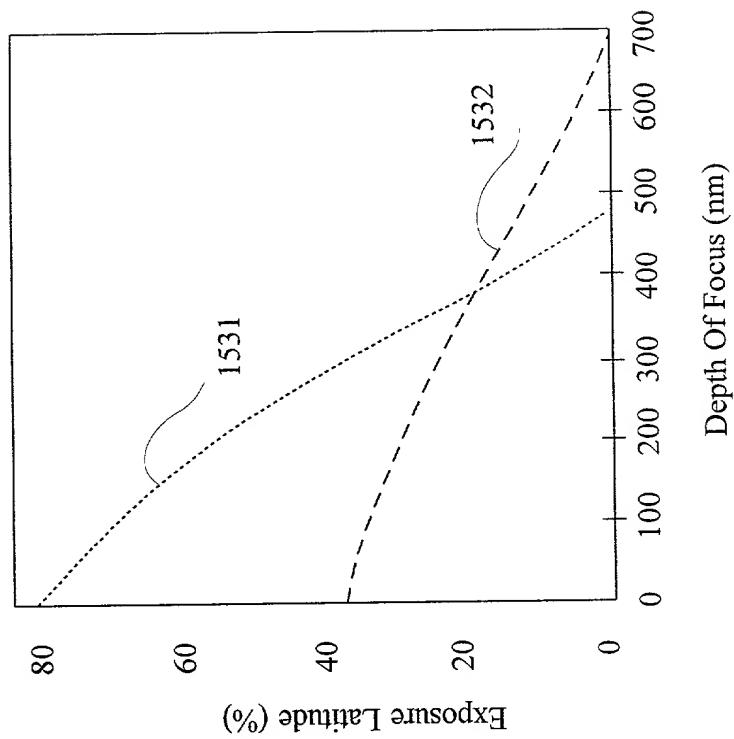


Figure 15D

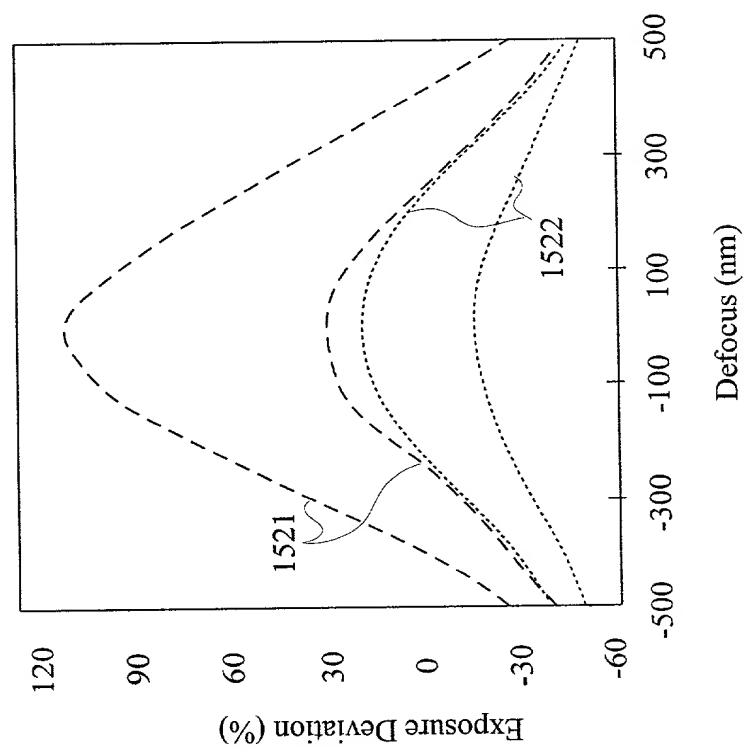


Figure 15C

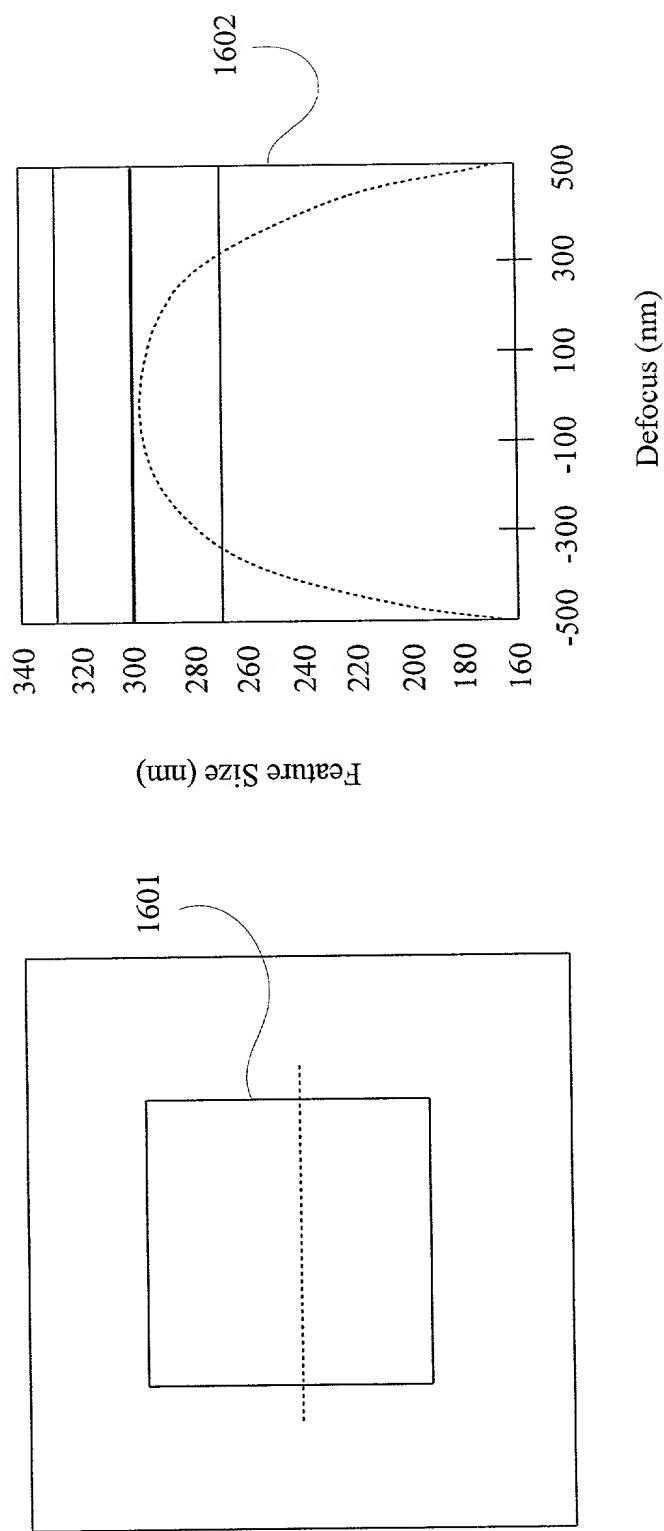


Figure 16A

Figure 16B

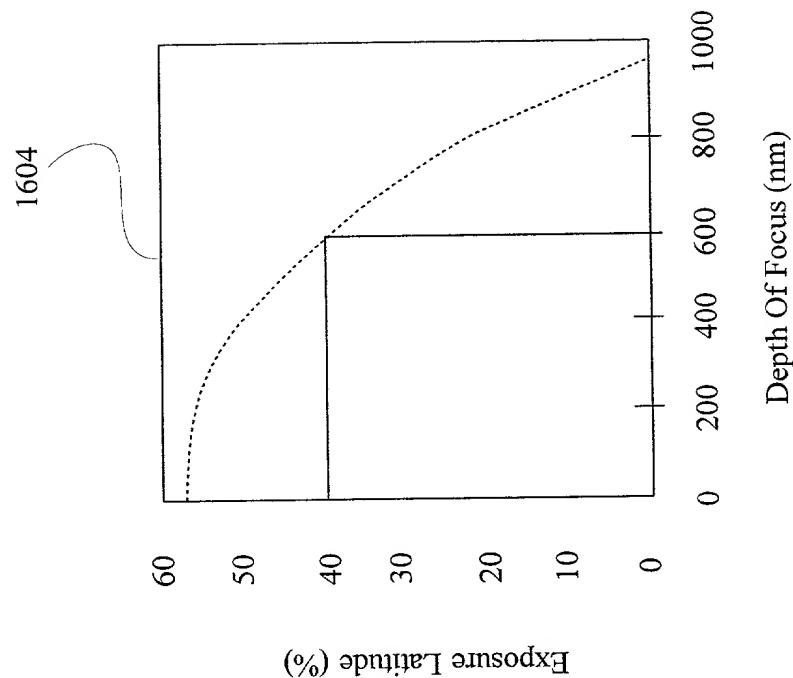


Figure 16D

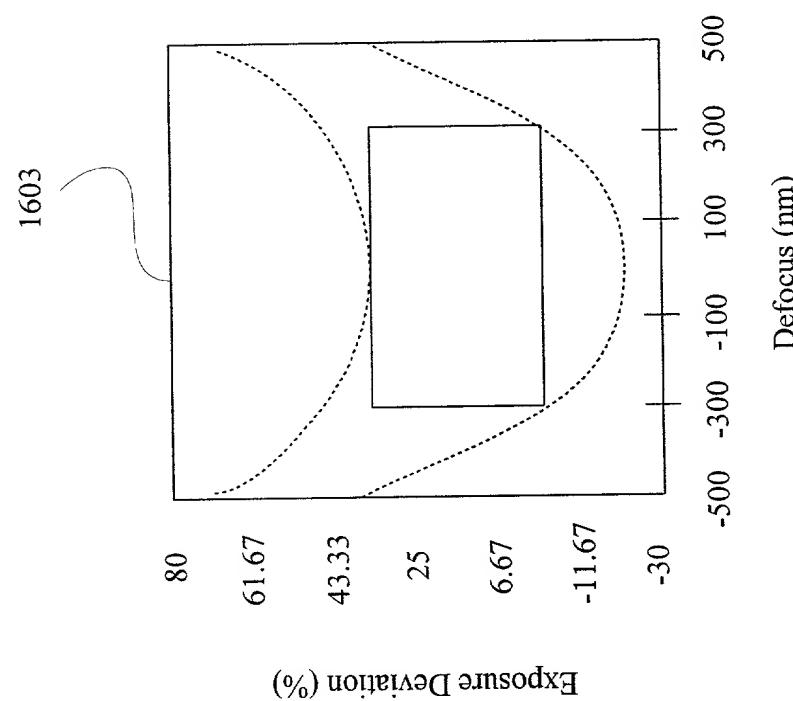


Figure 16C

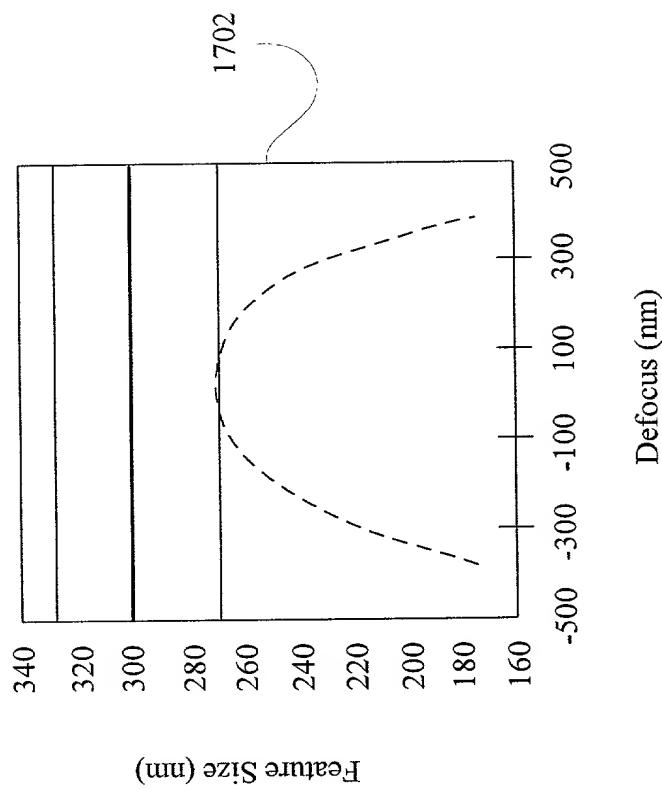


Figure 17B

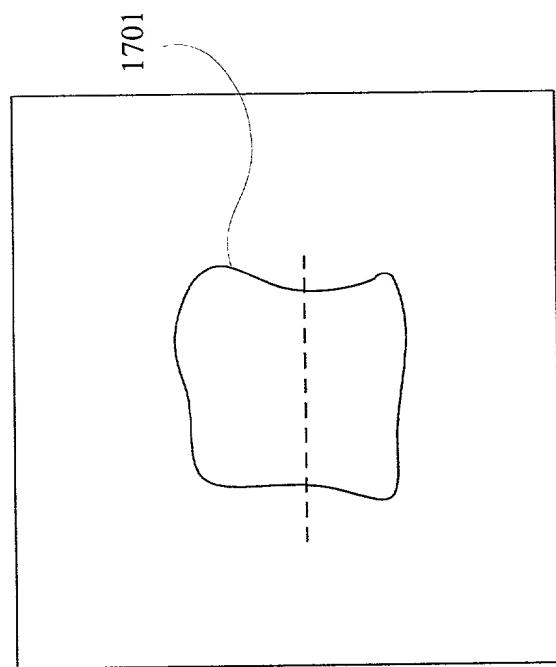


Figure 17A

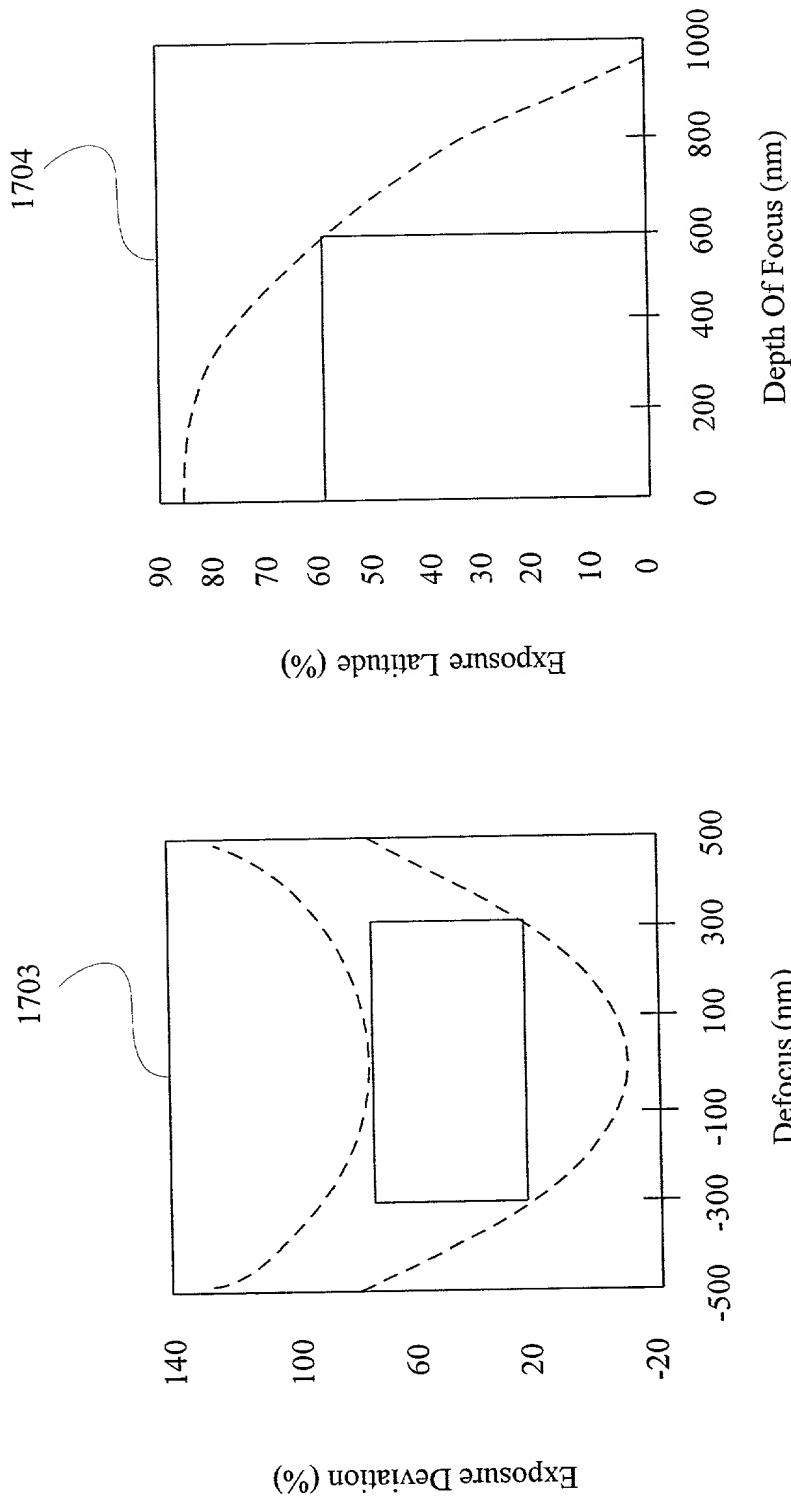


Figure 17C

Figure 17D

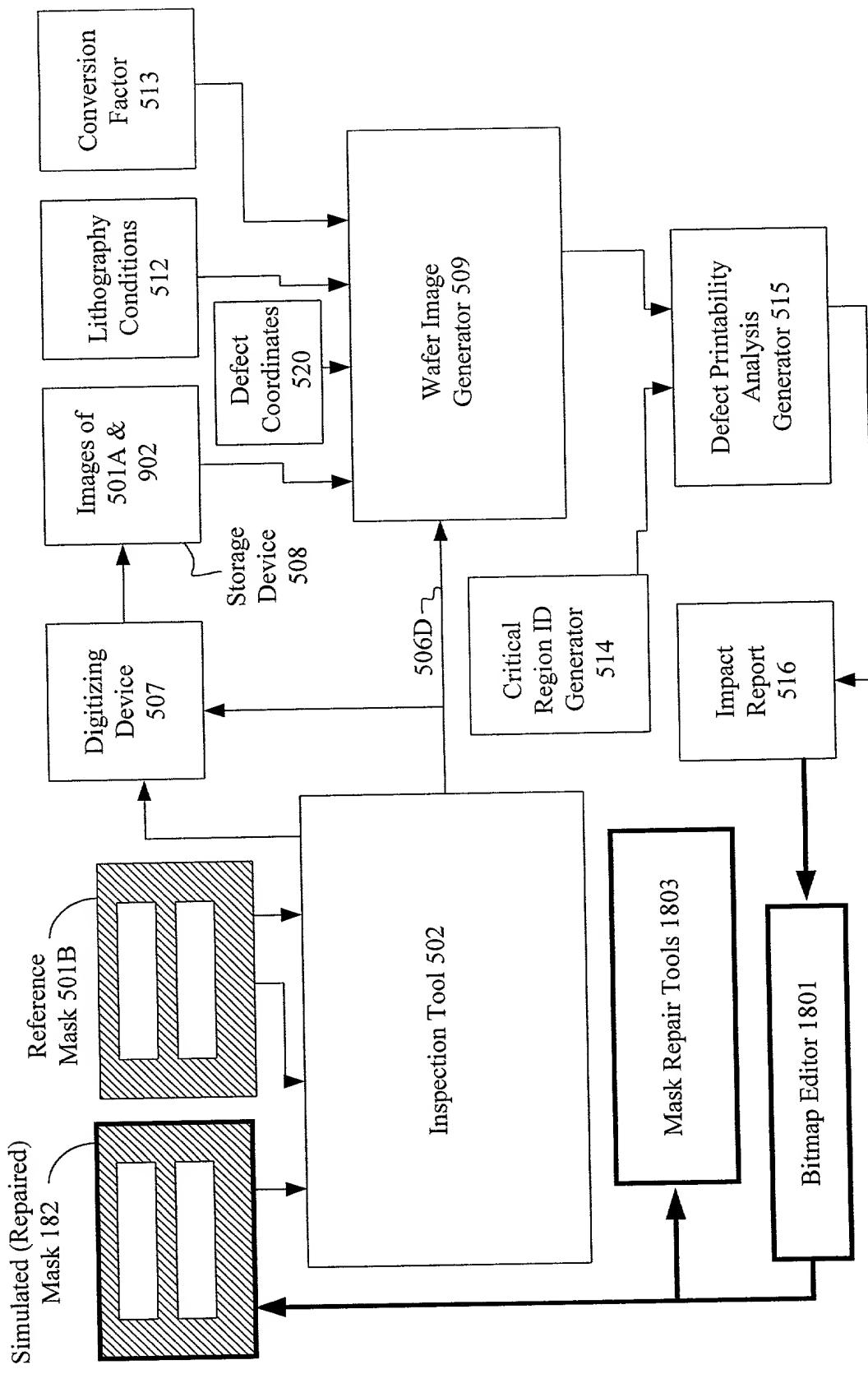


Figure 18

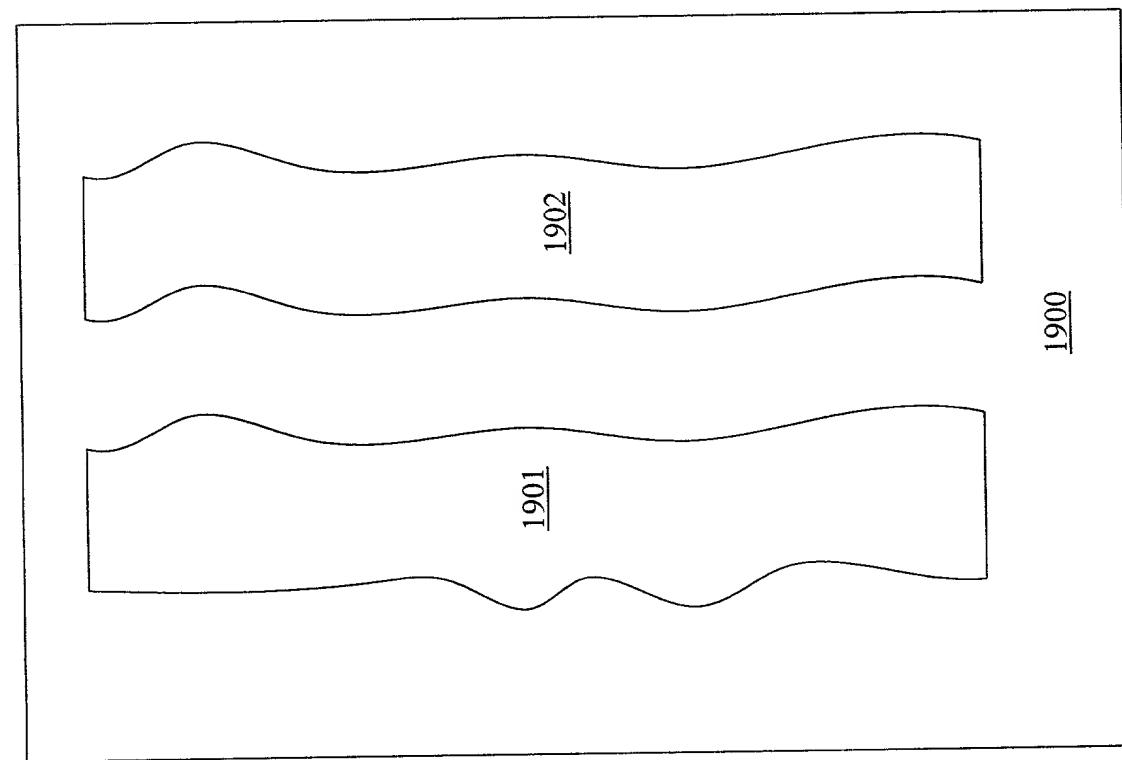


Figure 19A

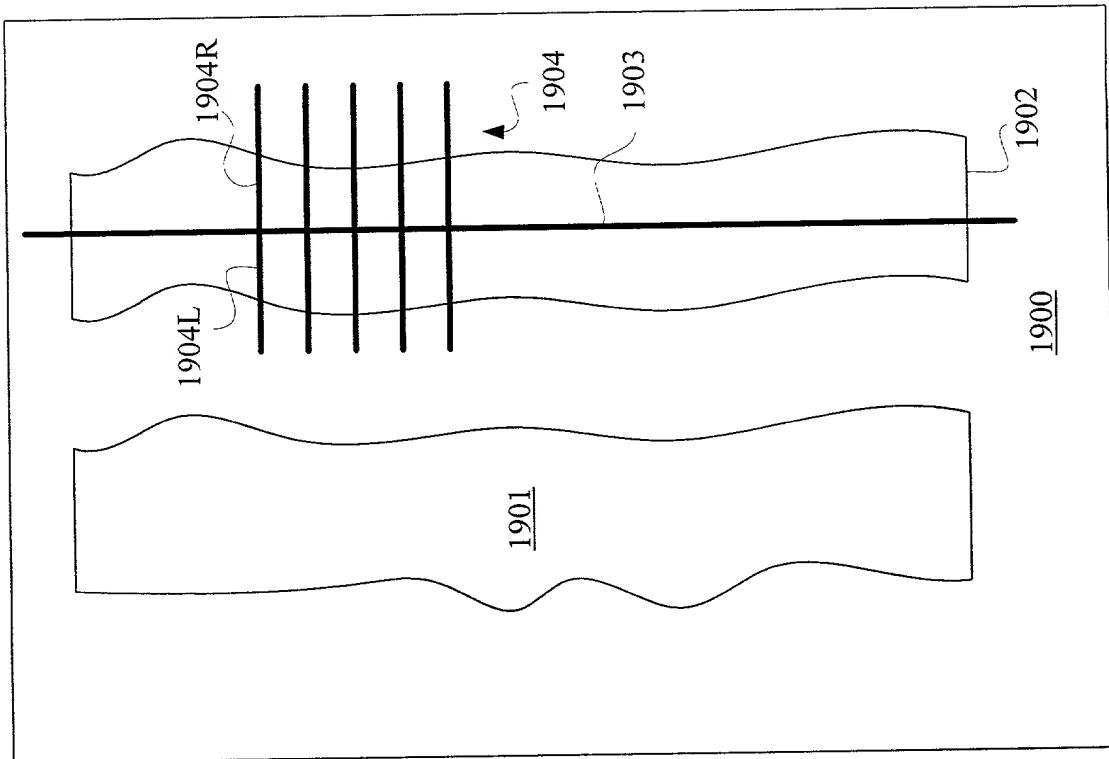


Figure 19B

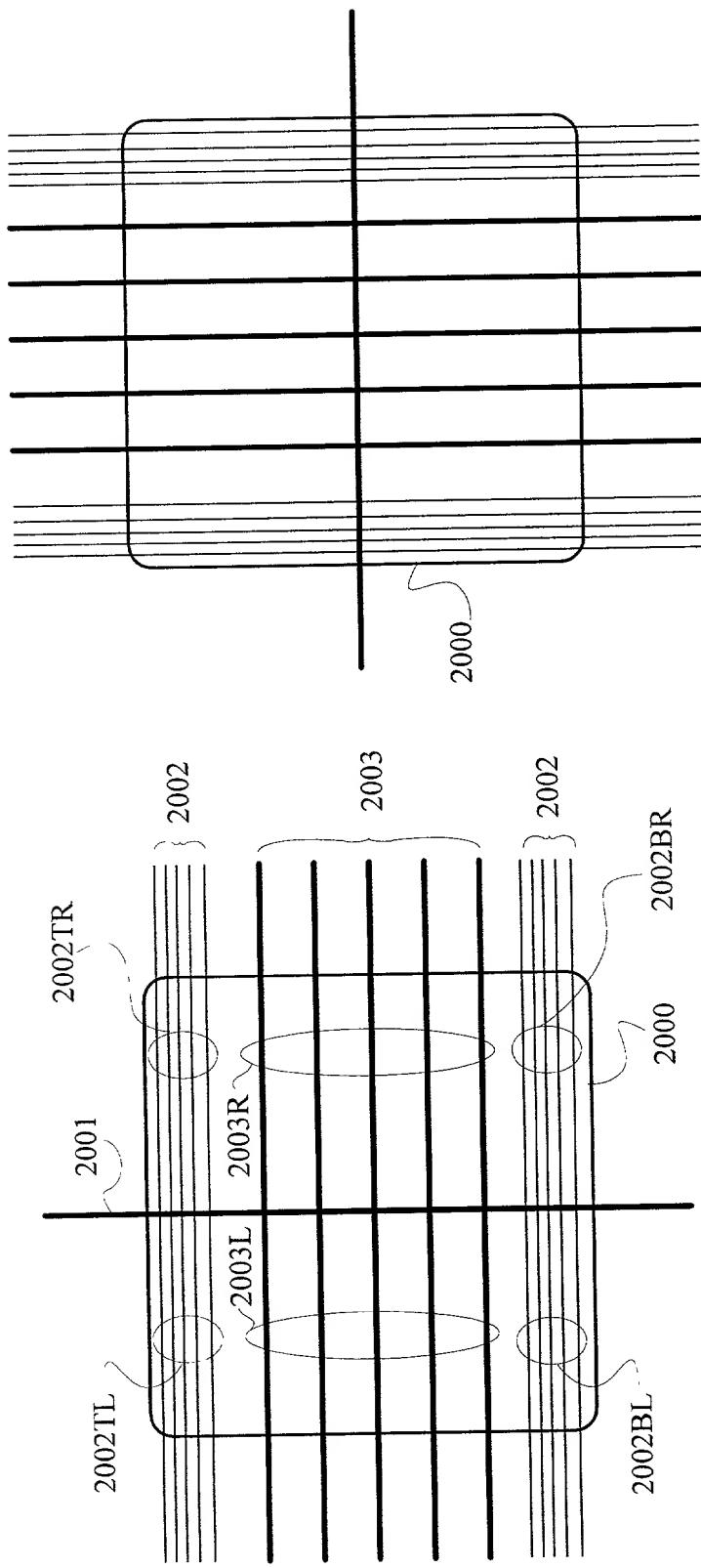


Figure 20A

Figure 20B